REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-14 are in this case. Claims 1-14 have been rejected under § 102(b). Claims 1-14 have been rejected under § 103(a). Dependent claim 5 has been amended. New claims 15-20 have been added.

The claims before the Examiner are directed toward a system in which a multiplicity of diverse dedicated hardware off-core execution units are connected to, but logically separate from, a core processor in order to increase the speed, power, and flexibility of the processor, and a method of operating the system. Reference instructions executed by the core processor initiate the execution of Configurable Long Instruction Word (CLIW) instructions stored in a CLIW memory. The operation of the off-core execution units is controlled by CLIW instructions. These CLIW instructions may also control operations performed by the core processor, and may be in addition to any other CLIW instructions that control the core processor exclusively. The off-core logic units are operationally connected to the data memory of the core processor under the control of the core processor's data address logic. The use of CLIW technology for the control of the off-core hardware logic units allows the addition of a plurality of diverse off-core logic units without affecting the instruction set, coding space, or instruction decoders of the core processor.

§ 102(b) and § 103(a) Rejections - Lavi et al. '922

The Examiner has rejected claims 1-14 under § 102(b) as being anticipated by Lavi et al., WO 99/42922 (henceforth, "Lavi et al. '922"), or, in the alternative, as obvious over Lavi et al. '922. The Examiner's rejection is respectfully traversed.

Lavi et al. '922 teach a processor that uses CLIW instructions to control computational units. While Figure 1 of Lavi et al. '922 does show a processor that includes several different parts, there is neither a hint nor a suggestion in Lavi et al. '922 of any utility to separating one or more of computational units (61, 62, 63, 64) from the rest of the system in an interchangeable fashion. The term "off-core" does not even occur in the text of Lavi et al. '922. While Figure 1 of Lavi et al. '922 does indeed show computational units (61, 62, 63, 64) as separate from the rest of the parts (1-5, 7-10, and 15) of the processor, that figure shows *all* of the parts (1-5, 7-10, and 15) of the processor as separate parts (The only exception is (see Lavi et al. '922, page 9, lines 28-29) means (8) for receiving a decoded instruction, which is shown there as embedded within execution logic unit (7). It is respectfully submitted that this last-mentioned exception is irrelevant to the matter at hand, being mentioned here only for the sake of completeness.) Thus, Figure 1 of Lavi et al. '922 does not indicate that there is any particular significance to the separation of computational units (61, 62, 63, 64) from the rest of the parts (1-5, 7-10, and 15) of the processor.

By contrast, referring to Figures 1 and 2 of the present application, the device of the present invention explicitly separates off-core execution units (54) from the rest of the processor. Note, especially, that in Figure 1 of the present application the off-core execution units (54) are shown as rectangles separated from the rectangle depicting the core processor (50), and that in Figure 2 of the present application all of the elements of the core processor (50) are shown enclosed within a broken-line boundary, and the off-core execution units (54) are shown outside the above-mentioned broken-line boundary.

It is respectfully submitted that the Examiner's characterizing computational units (61, 62, 63, 64) as off-core constitutes impermissible hindsight, in that the

advantage to this particular partitioning of the system is clear to one having knowledge of the present invention, but would not be obvious to one only having knowledge of Lavi et al. '922.

Although the decision of where to place the parts of a system is indeed a design choice, it is respectfully submitted that the making of advantageous design choices is a fundamental part of systems engineering, and that the present invention teaches such a choice, and that this choice is not made obvious by Lavi et. al '922. The flexibility, provided by the present invention, in adding new types of execution units (54) that had not even been conceived of at the time the core processor (50) was fabricated, represents a major technical and commercial advantage. The present invention allows a processor that was fabricated and packaged long ago, and has even been in service for a long time, to be upgraded with new hardware capabilities without modification of the core processor (50) or the instruction set of the core processor (50). This allows the continued use of "legacy" software alongside new software that makes use of the new hardware.

The present application states, page 3, lines 7 through 11:

> Figure 1 depicts the general principle of the present invention. External off-core processing units **54** are connected to a core processor **50** in an interchangeable and selectable manner by means of an interface **52**. This interchangeable selection of off-core processing units allows the core processor to be enhanced in processing power, speed, and flexibility in accordance with the needs of a particular application. (emphasis added)

The present application further states, page 3 line 20 through page 4 line 1:

> The exclusive use of CLIW instructions to control the operation of the off-core execution units has the advantage of allowing the addition of one or more off-core execution units of varying designs, which may not have even been conceived at the time of the design of the core processor, without requiring modification of the core processor, its instruction decoder, or its instruction set, since the control signals used to control the off-core execution units are derived

from the CLIW memory, and sent to the off-core execution units via the off-core-execution-unit interface. (emphasis added)

There is neither a hint nor a suggestion in Lavi et al. '922 of this sort of flexibility to add new execution units long after the core processor design has been frozen.

Thus, the claims of the above-identified patent application are allowable as submitted. Nevertheless, while continuing to traverse the Examiner's rejections, Applicant has, in order to expedite the prosecution, chosen to add dependent claims 15-20 in order to further distinguish the present invention from the device of Lavi et al. '922. Specifically, claims 15 and 18 have been added to clarify that the off-core execution units are separate from the core processor, claims 16 and 19 have been added to emphasize the ability of a processor according to the present invention to be connected to off-core execution units of various types in an interchangeable manner, and claims 17 and 20 have been added to emphasize the function of the off-core-execution-unit interface in providing a clean, simple mechanism for connecting disparate off-core execution units to the processor.

Support for these new claims can be found in the specification. Specifically, support for the separation of the off-core execution units from the core processor, as recited in claims 15 and 18, can be found in Figures 1 and 2 and in the above citation from page 3 lines 7-11.

New dependent claims 15 and 18 feature language which makes it absolutely clear that the device of the present invention separates the off-core execution units from the core processor in a manner that is not hinted at or suggested in Lavi et al. '922.

Support for new dependent claims 16 and 19 can be found in the above citation from page 3 lines 7-11.

Support for new dependent claims 17 and 20 can be found in Figures 1 and 2,

in the above citations from page 3 lines 7-11 and page 3 line 20 through page 4 line 1, and in the following citation from page 8 line 6 through page 9 line 1 of the present application:

> Refer now to Figure 2. CLIW instructions are invoked by means of reference instructions. The reference instruction is a regular instruction in the instruction set of core processor **50** which has the function of invoking CLIW instructions. The operation code portion of the reference instruction indicates to a regular instruction decoder **14** of the core processor that a CLIW instruction is to be processed. CLIW signal line **34** is set by regular instruction decoder **14** in accordance with whether the core processor instruction currently being processed is a regular instruction or a reference instruction. If the core processor instruction currently being processed is not a reference instruction, CLIW signal line **34** is cleared by regular instruction decoder **14**, so that output **40** of control multiplexer **16** is driven by output **36** of regular instruction decoder **14**, allowing normal processing of the instruction. However, if the core processor instruction currently being processed is a reference instruction, regular instruction decoder **14** passes to a CLIW memory **18** a portion of the reference instruction containing a pointer to the appropriate CLIW instruction contained in CLIW memory **18**. CLIW memory **18** is operative to send this CLIW instruction to a CLIW instruction decoder **20**, and CLIW signal line **34** is set by regular instruction decoder **14** so that output **40** of control multiplexer **16** is driven by output **38** of CLIW instruction decoder **20**. CLIW signal line **34** also activates an off-core-execution-unit interface **52**, causing off-core-execution-unit interface **52** to accept the portions of the decoded CLIW instruction relevant to off-core execution units **54** and pass them to off-core execution units **54** for execution. (emphasis added)

New dependent claims 16, 17, 19 and 20 feature language which makes it absolutely clear that the device of the present invention provides for selection and connection of off-core execution units in a manner that is not hinted at or suggested in Lavi et al. '922.

Applicant believes that the amendment of the claims completely overcomes the Examiner's rejections on § 102(b)/ § 103(a) grounds.

Other Amendments to the Claims

In claim 5, a comment that should have been edited out prior to submitting the original application has been removed.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1 and 6, and hence dependent claims 2-5 and 7-20 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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